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For

A METHOD FOR APERTURING VERTICAL-CAVITY SURFACE-EMITTING LASERS

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A METHOD FOR APERTURING VERTICAL-CAVITY SURFACE-EMITTING LASERS (VSCELs)? (VCSELs)

[0001] This invention was made with the support of the United States Government under Grant No. MDA972-98-1-0001, awarded by the Department of Defense (DARPA). The Government has certain rights in this invention under 35 U.S.C. §202.

[0002] The contents of this application are related to those provisional applications having serial numbers 60/227,165, 60/227,161, and 60/226,866, filed August 22, 2000, and a provisional application having serial number 60/262,541, filed January 16, 2001. The present application claims priority to these related provisional patent applications and their contents are hereby incorporated by reference in their entirety into the present disclosure. The contents of this application are also related to several nonprovisional patent applications being filed concurrently herewith. These nonprovisional patent applications are hereby incorporated by reference in their entirety and have the following attorney docket reference numerals: 510015-263, 510015-264, 510015-265, 510015-266, 510015-268, 510015-269, 510015-270, 510015-271, and 510015-272.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention:

[0004] The present invention relates to a surface emitting semiconductor laser and a method for manufacturing the same. Especially the present invention relates to a vertical-cavity surface-emitting semiconductor laser for long wavelengths (i.e., **1.3** to **1.55** μm) to be used as an optical source for a system of optical communication, optical interconnection, optical data-processing, or the like, in the field of optical data-communication or optical data-processing, and also to a method for manufacturing the novel vertical-cavity surface-emitting semiconductor lasers for long wavelengths.

[0005] 2. General Background:

[0006] Significant recent progress in the development of vertical-cavity surface-emitting lasers (VCSEL's) emitting at 1.3-1.55μm is quickly making these light sources a viable option as high-performance components for optical fiber networks. In addition to offering cost advantages through such features as on-wafer testing, VCSEL's also have inherent advantages over edge-emitters such as scalability to two-dimensional arrays. Although many of the best results for these devices have resulted from the wafer-fusion or metamorphic growth of AlGaAs-based distributed Bragg reflector (DBR) mirrors with InP-based active regions, there is still considerable interest in the monolithic growth of long-wavelength VCSEL's completely lattice-matched to InP. Essentially, lattice-matched, highly reflective AsSb-based DBRs eliminate the need for the complicated mirror schemes.

[0007] The mirror stacks are formed of multiple pairs of layers often referred to as mirror pairs. The pairs of layers are formed of a material system generally consisting of two materials having different indices of refraction and being easily lattice matched to the other portions of the VCSEL. For example, a GaAs based VCSEL typically uses an $Al_{x1}Ga_{1-x1}As\backslash Al_{x2}Ga_{1-x2}As$ material system wherein the different refractive index of each layer of a pair is achieved by altering the aluminum content x1 and x2 in the layers, more particularly the aluminum content x1 ranges from 0% to 50% and the aluminum content of x2 ranges from 50% to 100%. In conventional devices, the number of mirror pairs per stack may range from 20-40 pairs to achieve a high percentage of reflectivity, depending on the difference between the refractive indices of the layers. The large number of pairs increases the percentage of reflected light.

[0008] In summary, a VCSEL includes a first distributed Bragg reflector (DBR), also referred to as a mirror stack, formed on top of a substrate by semiconductor manufacturing techniques, an active region formed on top of the first mirror stack, and a second mirror stack formed on top of the active region. The VCSEL is driven by current forced through the active region.

SUMMARY OF THE INVENTION

[0009] Apertures in VCSEL's, both oxide and air, have been used extensively in VCSELs to confine the current to the center of the device and to define a waveguide that keeps the optical mode away from the etched side-walls of the device. These apertures, however, have always been placed away from the active region itself allowing carriers to spread either before they reach the active region or in the quantum wells themselves. This carrier spreading results in a scattering loss in the cavity along with an associated optical loss. Subsequently, these losses limit the reduction in threshold current and increase in the external quantum efficiency. Thus, what is needed is a method for manufacturing VCSEL's that further reduces the threshold current and further increases the external quantum efficiency.

[0010] Accordingly, in one embodiment of the present invention, a vertical-cavity surface-emitting laser (VCSEL) for increasing external quantum efficiency is comprised of a first reflecting surface (a first DBR), a second reflecting surface (second DBR), and an active region having a selectively etched aperture with a predetermined size. The aperture is etched into the active region to reduce loss due to scattering in a cavity of a VCSEL, thereby increasing external quantum efficiency of the VCSEL. A selective etch that controls the rate of etching of the active region in relation to the DBR's is applied to the active region and the DBR's. This selective or preferential etch substantially removes the active region of the VCSEL while leaving the DBRs substantially intact, thereby aperturing the current as well as the optical mode to the center of the VCSEL structure. This selective etch is preferably performed by a predetermined ratio of citric acid to hydrogen peroxide.

[0011] Accordingly, in another embodiment of the present invention, a vertical-cavity surface-emitting laser (VCSEL) for decreasing threshold current density comprises: (i) a first reflecting surface, (ii) a second reflecting surface, (iii) an active region with a first surface and a second surface, (iv) a first cladding layer between the first reflecting surface and the first surface of the active region, (v) a second cladding layer between the second reflecting surface and the second surface of the active region, (vi) an aperture formed by selectively etching the active region to a predetermined ratio of the size of the active region to the size of a DBR. The aperture is formed adjacent the active

region to reduce loss due to scattering in a cavity of a VCSEL, thereby decreasing threshold current density in the VCSEL. The VCSEL may also have a tunnel junction on the first surface of the active region.

[0012] Accordingly in another embodiment, specific etchants can be used to etch the active region, while simultaneously precluding etching of the cladding layers. This can be done by protecting the sidewalls of the reflecting mirrors with a dielectric coating and then etching the active region with the etchants.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] In order that the manner in which the above-recited advantages and objects of the invention are attained, as well as others which will become apparent, more particular description of the invention briefly summarized above may be had by reference to the specific embodiments thereof that are illustrated in the appended drawings. It is to be understood, however, that the appended drawings illustrate only typical embodiments of the invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0014] Fig. **1** depicts a schematic of the VCSEL which is grown by molecular beam epitaxy on an *n*-doped (Sn) InP substrate;

[0015] Fig. **2** depicts a schematic of the VCSEL which is grown by molecular beam epitaxy on an *n*-doped (Sn) InP substrate, further having a tunnel junction between the top InP cladding layer and the active region;

[0016] Fig. **3** shows a cross-sectional SEM micrograph view of a test VCSEL structure etched for 60 minutes in a mixture comprising of citric acid and hydrogen peroxide having a predetermined ratio of about 2.2:1;

[0017] Fig. **4** shows a plot representing the threshold current reduction with each etch as the aperture size defined by the underetch is also decreased;

[0018] Fig. **5** depicts the improvement in the external quantum efficiency with etching;

[0019] Fig. **6** shows the *L-I-V* from a 25μm diameter device and the *L-I-V* from the same device with a 5μm aperture, forming a 15μm device;

[0020] Fig. **7** shows a tapered aperturing scheme by having materials with different etch selectivities, the taper being formed on one side of the aperture;

[0021] Fig. **8** shows a tapered aperturing scheme by having materials with different etch selectivities, the taper being formed on both sides of the aperture; and

[0022] Fig. **9** depicts a plot of the etch rates of different alloys that are lattice matched to InP with an etchant comprising of hydrogen peroxide diluted citric acid.

[0023] Fig. **10** schematically illustrates a more general embodiment of the selective aperturing method of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0024] A schematic for the VCSEL structure is shown in Fig. **1**. The bottom DBR **1** and the top DBR **2** consist, respectively, of preferably twenty-three and thirty-two pairs of $Al_{a1}Ga_{1-a1}As_xSb_{1-x}$ and $Al_{a2}Ga_{1-a2}As_xSb_{1-x}$ ($a_1>0.9$, $a_2<0.3$, $x>0.5$) $\lambda/4$-layers, generally shown as **3,** lattice-matched to InP cladding layers **4**. Lattice-matching is achieved by using previously-calibrated group-V induced reflection high-energy electron diffraction oscillations and then growing at conditions with near-unity antimony incorporation rates. As an alternative, only the top cladding layer or the bottom cladding layer may be present in the VCSEL depicted in Fig. **1**. A small amount of Ga is generally added to the AlAsSb reflecting surfaces so as to stabilize these surfaces chemically, and make them more resistive to degradation without substantially increasing their index of refraction.

[0025] This method ensures both reproducibility of results without daily repetition of the calibrations and also reliability of lattice-matching throughout a single growth. Both the DBR mirrors are doped uniformly *n*-type with PbTe and have linearly graded interfaces between the low- and high-index layers. The doping level is chosen to be n~$1x10^{18}/cm^3$ in the AlAsSb near the cavity and n~$4x10^{18}/cm^3$ in the AlAsSb several periods (about two penetration lengths of the mode) away from the cavity.

[0026] In order to provide electron-hole conversion from the top *n*-mirror, a thin, heavily-doped tunnel junction **5**, using CBr_4 as the *p*-type dopant and Si as the *n*-type dopant, may be placed at a standing-wave null of the mode in the cavity (shown in Fig. **2**, but not in Fig. **1**). Holes are created by extraction of electrons from the valence band

of the *p*-type layer in the tunnel junction. By using two *n*-type DBRs and placing the heavily-doped tunnel junction at a standing-wave null, the optical loss in this structure is minimized.

[0027] In another embodiment, conduction through one or both of the mirrors can be avoided by doping the thick InP cladding layers to serve as contact layers in a double-intracavity design. In this case, an electrical connection is made to one or both of the cladding layers. Using the tunnel junction **5** allows for the use of *n*-type contact layers which have both higher electrical conductivity and lower optical loss than similarly-doped *p*-type layers.

[0028] The cavity has an optical thickness of 1-λ and is grown entirely in the lattice-matched InAlGaAs system. Five strain-compensated InAlGaAs quantum wells, which have a large conduction band offset and are therefore promising for high temperature performance, are used as the active region **6**. A thin (50Å), heavily-doped layer of lattice-matched InGaAs is grown after the final mirror period to provide a better contact layer.

[0029] The structure, depicted in Fig. **1**, is fabricated into devices of diameters 10 to 100μm by Cl_2 reactive ion etching using a combination of the top TiPtAu contact and SrF_x as an etch mask. Contact to the bottom is made through the substrate using a broad-area NiAuGe contact. The active region **6** of the device is etched by a mixture that preferably uses citric acid and hydrogen peroxide. The etch is highly selective over a range of chemistries, with selectivity almost 100:1 existing between the active region and both the DBRs and InP substrate.

[0030] Alternatively, specific etchants such as H_3PO_4, or H_2O_2, or any combination thereof can be used to etch the active region, while simultaneously precluding etching of the cladding layers. This can be done by protecting the sidewalls 10a and/or 10b of the reflecting mirrors with a dielectric coating and then etching the active region with the etchants.

[0031] A cross-sectional SEM micrograph of a test VCSEL structure etched for 60 minutes in $CH_3COOH:H_2O_2::2.2:1$ is shown in Fig. **3**. Alternatively, the etch ratio of citric acid to hydrogen peroxide may be about 3:1, and the etching mixture may contain

compounds in addition to the citric acid and the hydrogen peroxide. The active region has been undercut by over 6μm. The AlAsSb-based DBRs, however, have not been etched significantly during this period. No protection is placed on top of the structure, but all the mirror periods are still visible. Citric acid, when diluted with hydrogen peroxide, etches InAlGaAs compounds much faster than both InP and AlGaAsSb compounds.

[0032] The arrow-like shape of the undercut tip is produced by a combination of two factors. First, the higher InGaAs composition of the quantum wells caused a slightly higher etch rate in the center of the cavity. Additionally, the exposed AlAsSb layers that directly clad the active region have oxidized and expanded, manifesting as thicker layers away from the tip and providing the small lip that is seen.

[0033] Using this same etch chemistry, a set of processed 50μm diameter VCSELs were repeatedly etched and tested after each etch. The etch depth is calibrated by etching test samples at the same time and additionally by cross-sectional SEM of non-VCSEL structures on the laser samples. The strong selectivity of the etch allowed the finished lasers to be etched without damaging the AlGaAsSb/AlAsSb DBRs.

[0034] As shown in Fig. **4**, the threshold current decreases with each etch as the aperture size defined by the underetch is also decreased, reaching a minimum of 13mA for a 33μm device (50μm pillar with 8.5μm undercut). For example, a 50 micron device has a threshold current of about 30mA, whereas after etching, a 46.5 micron device has a threshold current of about 22 mA. This corresponds to a reduction in threshold current by about 26%. The threshold current density is relatively constant during these etches, decreasing slightly initially as the optical loss is reduced. The reverse current also decreases slightly during this process, indicating no leakage currents are being introduced.

[0035] The external quantum efficiency for these lasers is plotted in Fig. **5**. The efficiency improves with etching, rising to 13%. For example, a 50 micron device has a quantum efficiency of about 9%, whereas after etching, a 46.5 micron device has a quantum efficiency of about 10%. This corresponds to an increase in quantum efficiency by about 11%. This improvement indicates a reduction in optical loss as the aperture

confines the mode away from the etched sidewalls and therefore reduces the scattering associated with these rough surfaces.

[0036] Another important benefit of this aperturing technique, however, is the ability to decrease the active area while maintaining a constant contact area. This reduces the power consumed by the device and therefore limits the heating in the active region. Since the thermal conductivity of the AsSb-based DBRs is very low, this minimization of the power is very important to device performance.

[0037] Fig. **6** shows the *L-I-V* from a 25μm diameter device and the *L-I-V* from the same device with a 5μm aperture, forming a 15μm device. The threshold current has been reduced by more than half from 6.1mA to 2.8mA, which does correspond to a slight increase in threshold current density from 1.2kA/cm^2 to 1.6kA/cm^2. However, the threshold voltage is relatively unchanged, so the dissipated power for this device at threshold has been reduced from 35.8mW to 16mW, demonstrating the benefit of aperturing these devices. Additionally, the external quantum efficiency has increased slightly, again implying that the aperturing decreases the optical loss in the structure.

[0038] The threshold current of lasers to which this etch is applied decreases with each etch as the aperture size defined by the underetch is also decreased. The current density is seen to decrease slightly for the initial etches and the external quantum efficiency also improves, demonstrating the beneficial aperturing effects of the undercut.

[0039] In another embodiment of the present invention, a device 100, 200 is apertured by selectively etching an aperture 110, 210 between a first 226 and a second surface 124, 224. At least one of the surfaces is tapered as shown in FIGs. **7** and **8**. By properly choosing the materials, based on the selectivity of etching, within the aperture and within the adjacent surfaces 124, 224, 226 it is possible to etch the aperture 110, 210 at a rate substantially faster than the adjacent surfaces to provide tapering. Thus, the material of the surfaces is etched vertically as well as laterally. The tapered surfaces can be very beneficial to the VCSEL design by providing an optical lens for focusing the light into the active region 110, 210.

[0040] The aperture schemes of Figs. **7** and **8** can utilize an InAlGaAs active region **110**, **210** along with InP cladding layers **120**, **122**, **220**, **222**. The tapered surfaces **124**,

224, can be formed of InAlAs, for example. The InAlAs can serve as a barrier layer for the quantum wells of the active region **110**, **210**. The InAlAs can also serve as part of the tunnel junction **5** of Fig. **2**.

[0041] Fig. **9** illustrates the different etch rates for different materials and various dilutions of the etchant $CH_3COOH:H_2O_2$. Looking at the etch rates for the different materials for an etchant ratio of unity, it can be seen that InP is at approximately 10, InAlAs is at approximately 40 and InGaAs is at approximately 900. InGaAs typically is not used as an aperture by itself because it is absorbing, it has the lowest band gap. The alloy InAlGaAs which can be used in the aperture, is not illustrated in the plot, but would lie somewhere between the plot for InAlAs and InGaAs. Both the InAlGaAs and InAlAs are very selective (etched rapidly) compared to InP. Selective etch of InGaAs is clearly obtained comparing to the other systems lattice-matched to InP such as InAlAs and GaAsSb. The selectivity of about 30:1 between InGaAs and InAlAs implies that no significant difference between the materials is really needed. Nevertheless the best selectivities are achieved with alloys having larger discrepancy of the atomic composition. The best selectivity of 143:1 has been obtained between InGaAs and GaAsSb. Thus, this selectivity based etching finds important usage in aperturing VCSELs. Thus, the InAlAs of the tapered surfaces is etched faster than the InP of the cladding layers but much more slowly than the InAlGaAs active region, resulting in the tapered surfaces. Adding more Ga to the InAlGaAs tends to result in even faster etching of the active region relative to the other regions. Ga can also be added to the InAlAs to provide faster etching of the surfaces 124, 226, 224. However, Ga is usually not added to the InAlAs when the InAlAs is to be used as part of the tunnel junction **5** because the electrical conductivity of the tunnel junction is better with InAlAs rather than a quaternary material. By using different alloy compositions, and different etching chemicals and dilutions, this approach allows the tuning of the selectivity. $Al_xIn_{1-x-y}Ga_yAs$ alloys can be used for this purpose. A direct application of this technique is to generate tapered apertures by using a composition grading. Different dilutions of the etching chemicals will provide different aperture angles.

[0042] This selective etch aperturing method is useful in in-plane semiconductor laser diodes, heterostructure bipolar transistors (HBT) and VCSELS, as well as other devices where an aperture is useful for confining current and/or an optical mode.

[0043] In general the an aperture is formed by selective etching (meaning etching different materials at different rates) of a material substantially lattice matched to InP, or similar material, relative to layers of InP, or similar material, between which it is sandwiched. The etched material can include As combined with group V materials such as B, Al, Ga, In, or Ti. The etched layer does not necessarily need to be the active region, but it can be the active region since the active region is composed of materials that can be substantially lattice matched to InP. The etched layer, for example, can be a layer of InAlAs or InAlGaAs, both of which can be substantially lattice matched to InP. This selective etching can be used to form apertures between InP layers in VCSELs. Where the active region is composed of As materials, the selective etching can be used to etch the active region.

[0044] Fig. **10** schematically illustrates a more general embodiment of the selective aperturing method of the present invention. A VCSEL **300** has a substrate **302**, mirrors **304**, InP layers **306**, **308**, **310**, and active region **312** also illustrated is an aperture **314** and tapered surface **316**. In the general embodiment the aperture does not need to be formed in the active region. One or more apertures can be formed between any two InP layers. The aperture **314** can be composed of a material lattice matched to InP, typically a material composed of As, such as InAlGaAs or InAlAs. The aperture **314** material should have a relatively high selectivity, or etching rate, relative to InP. Fig. **10** shows two apertures **312**, **314**, wherein the aperture **312** is also the active region. In some embodiments, one aperture can serve to confine the current while another serves to confine the optical mode. Any of the apertures can include a composition grading to achieve different tapering angles. Fig. **10**, for example, includes a tapered surface of InAlAs or InAlGaAs (having a lower Ga content than does the section **314** of the aperture) which will etch slower than the InAlGaAs aperture **314**. The material of the aperture **314** should be lattice matched to InP and have a greater selectivity than InP when etched by the etchant. Many layers of apertures sandwiched between layers of InP can be created by alternatively etching through an InP layer without significantly

etching the As containing layer, next etching the As containing aperture layer without significantly etching the InP layer, and then starting the process again by etching through the next InP layer without significantly etching the next As containing layer. The tunnel junction, if included, should be adjacent the active region.

[0045] The present embodiment is not limited to InP, but rather, other similar materials with similar properties can be substituted.

[0046] In a nutshell, unlike shorter-wavelength AlGaAs-based VCSELs, there is no natural oxidizable material in an InP-based monolithic VCSEL from which an oxide aperture can be formed. By taking advantage of the different materials used in AlAsSb-based VCSEL's, however, a selective etch can be used to partially remove the InAlGaAs-based active region 6 while precluding substantial etching of the AlGaAsSb-based DBRs **4**. This aperturing thereby confines the current and the mode to the center of the structure. Furthermore, this scheme of selectively etching the active region at a rate faster than the rate of etching of the DBR's produces an aperture of increasing size. This helps eliminate some sidewall scattering loss and, therefore, lowers the threshold current density and increases the external quantum efficiency of the VCSEL.

[0047] While the specification describes particular embodiments of the present invention, those of ordinary skill can devise variations of the present invention without departing from the inventive concept. For example, the mixture may be designed in a manner to control the etch rate of the active region in a specific fashion. Furthermore, the mixture may also have different compositions in differing ratios. Other etchants such as H_3PO_4, H_2O_2 or their combinations may also be used.